

# PreDAC

PRECISION multi-channel  
Digital to Analog Converter



## User's Manual



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## **Safety information - Warnings**

CAEN ELS will repair or replace any product within the guarantee period if the Guarantor declares that the product is defective due to workmanship or materials and has not been caused by mishandling, negligence on behalf of the User, accident or any abnormal conditions or operations.

**Please read carefully the manual before operating any part of the instrument**



### **Do NOT open the boxes**

**CAEN ELS d.o.o. declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly this User's Manual before any kind of operation.**

CAEN ELS d.o.o. reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice.

### **Disposal of the Product**

The product must never be dumped in the Municipal Waste. Please check your local regulations for disposal of electronics products.



Read over the instruction manual carefully before using the instrument. The following precautions should be strictly observed before using the PreDAC device:

---

**WARNING**

- Do not use this product in any manner not specified by the manufacturer. The protective features of this product may be impaired if it is used in a manner not specified in this manual.
- Do not use the device if it is damaged. Before you use the device, inspect the instrument for possible cracks or breaks before each use.
- Do not operate the device around explosives gas, vapor or dust.
- Always use the device with the cables provided.
- Turn off the device before establishing any connection.
- Do not operate the device with the cover removed or loosened.
- Do not install substitute parts or perform any unauthorized modification to the product.
- Return the product to the manufacturer for service and repair to ensure that safety features are maintained

---

**CAUTION**

- This instrument is designed for indoor use and in area with low condensation.

The following table shows the general environmental requirements for a correct operation of the instrument:

<b>Environmental Conditions</b>	<b>Requirements</b>
Operating Temperature	0°C to 45°C
Operating Humidity	30% to 85% RH (non-condensing)
Storage Temperature	-10°C to 60°C
Storage Humidity	5% to 90% RH (non-condensing)





# 1. Introduction

This chapter describes the general characteristics and main features of the PreDAC Multi-channel Digital to Analog Converter.

## 1.1 The PreDAC - Digital to Analog Converter

The PreDAC Multi-channel Digital to Analog Converter by CAEN ELS is a (up to) 4-channel, 21-bit resolution, wide-bandwidth Digital to Analog Converter (DAC) which is especially designed for operation with the BEST (Beamline Enhanced Stabilization Technology) system.

The core of the PreDAC system is formed of high-speed 16-bit digital to analog converter that uses dithering technique and active low-pass filtering to obtain stable high accuracy (21-bit) output signal.

This device is capable of outputting  $\pm 12$  V bipolar voltage with resolution of 12  $\mu$ V – i.e. 21 bits of resolution on the bipolar output range. Output voltage noise is suppressed using a 4<sup>th</sup> order active low-pass filter with cut-off frequency (-3 dB) of 10 kHz. Low temperature drifts, good linearity and very low noise levels enable users to perform high-precision voltage signal generation.

The PreDAC is typically fitted with two output channels but can be optionally upgraded to have three or even four output channels. It is housed in a light, robust and extremely compact metallic box that can be placed as close as possible to the actuator power driver in order to reduce cable lengths and minimize possible noise pick-up. It is specially suited for applications where multi-channel simultaneous actuations are required, a typical application being the control of position (X, Y) and intensity ( $I_0$ ) of the photon beam in synchrotron radiation X-ray beamlines.

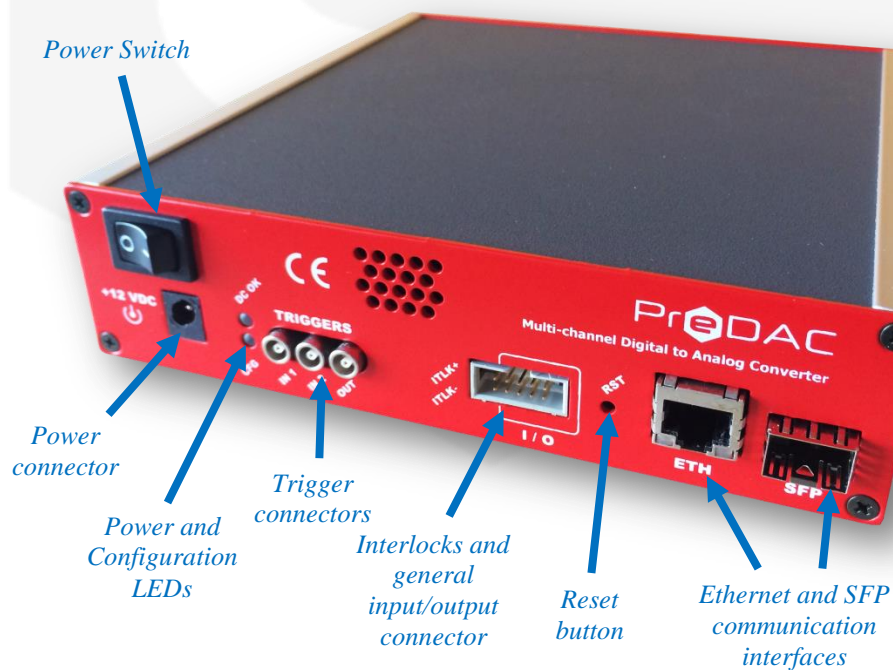
The PreDAC communication to a host PC is guaranteed by a standard 10/100/1000 Mbps Ethernet TCP/IP protocol while its integration in the BEST (Beamline Enhanced Stabilization Technology) system is performed via the SFP link present on the rear panel.

## 1.2 The PreDAC at a Glance

The PreDAC unit and its I/O connections can be easily seen in **Figure 1** (front) and in **Figure 2** (rear).



**Figure 1:** front view of a PreDAC unit



**Figure 2:** rear view of a PreDAC unit

There are up to four BNC connectors for outputting the analog voltages and various status LEDs placed on the front panel of the PreDAC unit. The total number of BNC connectors depends on the configuration of the PreDAC unit (default: two channels).

The two white LEDs on the front panel: the left one is the **ON** LED and it is turned on when at least one of the output channels is feeding the voltage to its corresponding connector. The other white LED is marked with **CL** (Closed Loop) and can be found on the rightmost side of the front panel. When lit up is indicating that the PreDAC is working in conjunction with the BEST system in the closed loop for beam stabilization.

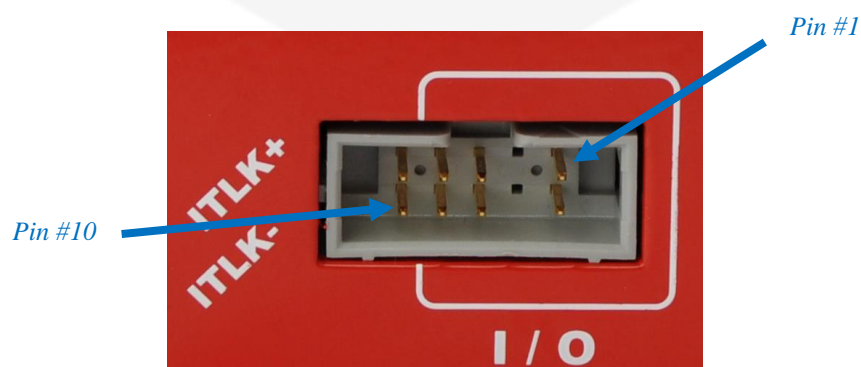
A blue **STATUS** LED, which is used to signal the correct operation of the PreDAC device, is also visible from the front panel. During normal operation of the PreDAC unit the **STATUS** LED is blinking with a frequency of 0.5Hz – i.e. the LED changes its status every 2 seconds; if a fault condition arises, the LED blinks with a higher frequency of 2 Hz (the led changes its status every 0.5 seconds). During the boot phase of the PreDAC unit (which takes about 12 seconds after a power cycle or hardware reset) all LEDs are turned on.

The power connector, power switch, two LEDs, LEMO connectors for I/O triggers, interlock and general I/O connector, a standard RJ45 Ethernet connector and an SFP connector are placed on the rear panel of the device.

The blue **CFG** LED indicates that the on-board FPGA is correctly configured (in this case the LED is turned on). The green **DC OK** LED indicates that the internal sections are correctly powered on.

The three coaxial LEMO connectors for I/O triggers are also placed on the rear panel. Please note that only the **IN 1** signal is enabled and can be used for a synchronized voltage output (see the Triggers Connector section). The other two connectors – i.e. **IN 2** and **OUT** – are reserved for future use.

The “Interlocks and general I/O connector” has the pinout configuration shown in **Figure 3**:



**Figure 3:** Interlock and general I/O connector

Pin #	Function
1-2	Reserved
3-4	Not present
5-8	General purpose I/O
9-10	External interlock

The external interlock pins can be used to detect an external event, which can be used to trigger the external interlock fault and to switch the present voltage outputs to a zero level (see Interlock and general I/O connector section for more information).

Please note that these interlock pins are galvanically isolated from ground.

The General purpose I/O pins are not yet used and they are reserved for future use on the device.

On the rear panel of the PreDAC there is a small hole that gives access to a reset button (“RST”), which can be used to reset the unit. Next to the reset button are placed a RJ45 Ethernet connector (“ETH”), which is used to communicate with the unit and a Small form-factor pluggable transceiver (“SFP”) which will be used for future updates.

## 1.3 Features

A host PC is necessary in order to operate the PreDAC unit and properly set/check the desired parameters (e.g. output voltage).

Please refer to the [Software commands](#) chapter for a complete description of available commands, their purposes and their syntax.

## 1.4 Offset calibration

The PreDAC device is already factory-calibrated during the production process. Gain and offsets are stored in the non-volatile internal memory.

However, user can perform an additional calibration – i.e. a *User Defined Calibration* – for example for nulling application specific offsets.

## 1.5 Dithering

Internal dither frequency for each channel is fixed to 100 kHz. This enables to achieve 21 bits of resolution in the standard operation mode (the minimum step size equals 12  $\mu\text{V}$ ).

The noise introduced by the dithering process is suppressed with active filtering. The fourth-order active filtering have 80 dB roll-off so the dithering noise is extensively damped.

In addition to this standard operation mode it is also possible to have the output voltage without the use of the dithering: the output voltage resolution is reduced to 16 bits (minimum step size equals 366  $\mu\text{V}$ ) even if the dithering noise is not present.

## 2. Software commands

This chapter describes the software commands used for the correct configuration of the PreDAC Digital to Analog Converter and for its data readout.

For more information about the Ethernet settings see the Ethernet Communication chapter.

### 2.1 Command Syntax

The command structure and syntax used by the PreDAC protocol are described in the following sections.

Commands must be sent in ASCII format and are composed by:

- one “*command field*”
- none, one or two “*parameter field*”

Please note that these fields are separated by a colon (‘:’ or ‘0x3A’ in hexadecimal notation). The number of “*parameter fields*” depends on the specific command.

All commands are **NOT case sensitive** and therefore the command string can be sent either using uppercase or lowercase characters (conversion to uppercase characters is performed internally).

Each instruction must be terminated with a ‘*carriage return\line feed*’ sequence ‘*r|n*’ (or ‘0x0D 0x0A’ in hexadecimal notation or commonly CRLF).

**Command Example:**

**RNG:1|r|n**

- “**RNG**” is the command field;
- ‘:’ is the parameter’s separation character;
- ‘1’ is the first parameter field;
- ‘|r|n’ are the termination sequence of the command.

Commands are processed one at a time; therefore user must wait for a response from the unit before sending the next command. All the responses from the PreDAC device are in upper case and are terminated with the same ‘carriage return\line feed’ sequence (‘|r|n’) – i.e. CRLF – used in the command.

The reply from the device depends on the given command; for more information about the single command please refer to the specific command section.

There are two specific replies that are commonly used in many commands, and that indicate that the command has been correctly elaborated or not. These replies are hereafter presented:

- **ACK**nowledge (‘**ACK**’) indicates that the command is valid and it was correctly elaborated by the device:

**ACK|r|n**

- “**ACK**” is the **ACK**nowledgement response to a valid command;
  - ‘|r|n’ is the termination sequence of the reply.
- **Not AcK**nowledge (‘**NAK**’) indicates that the command is either not valid or that it was not accepted by the device; the “**NAK**” reply is followed by an “error code” field, which can be used to determine the cause of the error (see the List of the Error Codes appendix for a detailed list of all possible error codes):

**NAK:nn|r|n**

- “**NAK**” is the **Not AcK**nowledged response to an invalid command;
- ‘:’ is the parameter’s separation character;
- ‘nn’ is a the number of the error code;
- ‘|r|n’ is the termination sequence of the reply.

The list of commands used by the PreDAC and the corresponding syntax is hereafter presented as well as a description of each command purpose and any special requirements related to the specific command. The commands are hereafter described and are grouped in categories based on their purpose.

## 2.2 Voltage Output Commands

The Voltage Output commands, used in order to set output voltage on one or all channels of the PreDAC device, are described in the following section.

### 2.2.1 SET Command

The PreDAC output voltage can be set by the means of SET command. Output voltage can be set separately for each channel or on all channels at one time.

The correct format for the SET command is as follows:

SET:*channel*:*value*\r\n

where:

- *channel* is the channel number (or all);
- *value* is the voltage output value (in [V]);

The *channel* parameter can be chosen between these values:

- "CH1" for the channel 1;
- "CH2" for the channel 2;
- "CH3" for the channel 3;
- "CH4" for the channel 4;
- "ALL" for the concurrent write of the same value to all channels.

The *value* parameter is defined as the output voltage to be set (in [V]). The *value* field is concatenated from the following subfields:

±XX.YYYYYYY

- "±" field for the number sign: "+" or "-";
- "XX" for the tens and units of the value;
- "." is decimal delimiter;
- "YYYYYY" for decimal places.

If more decimal places than the PreDAC resolution are sent to the unit, the value is rounded to the closest actable one and additional places are discarded. The resolution of the output voltage can be set with the RES command, which is described in the section 2.3.8 RES Command.

The *value* field can also have two other values:

- "OFF" to set zero voltage on the selected channel/channels;
- "?" for the readback of the set voltage on the selected channel/channels.



**Examples:**

*SET output voltage to 2.123456 V on all channels example:*

SET:ALL:+2.123456\textcolor{red}{r}\textcolor{red}{n}

ACK $\backslash r \backslash n$

*SET read on channel 2 example:*

SET:CHN2:?\textcolor{red}{r}\textcolor{red}{n}

SET:CH2:-11.123456\textcolor{red}{r}\textcolor{red}{n}

*SET zero voltage on channel 3 example:*

SET:CH3:OFF\(*r*\(*n*)

ACK $\backslash r \backslash n$

## 2.2.2 TRG Command

The TRG Command enables to synchronize the PreDAC output voltage setting to an external event via the hardware “Trigger/Gate” signal (refer to the Triggers Connector section). This feature is extremely useful when the digital to analog converter must be synchronized to an external event (e.g. an experimental time window or a machine specific frequency).

In the **normal mode** the execution of the SET command reflects in the immediate change of the output voltage value. In the **trigger mode**, on the other hand, the execution of the SET command does not get into operation immediately. The output voltage value which is set with the SET commands is saved into memory (on a temporary register): when the external signal occurs it forces the change of the output voltage setting. The **trigger mode** operation is hereafter described.

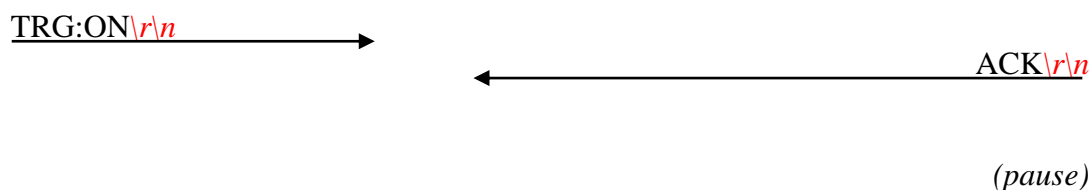
As soon as the “TRG:ON\r\n” command is received the PreDAC unit replies with an acknowledgement string (“ACK\r\n”) and enters the **trigger mode**. When entering this mode, the unit waits for a rising edge (positive edge) on the corresponding “Trigger/Gate” input signal. As soon as this event is detected by the PreDAC unit, the internal logic transfers the output voltage value from the temporary register to the output register which results in the output voltage update on the BNC output connectors. This behavior is kept until the **trigger mode** is disabled with the “TRG:OFF\r\n” (*default*) command. Please note that an acknowledgment string is sent back to the host after a “TRG:ON\r\n” or “TRG:OFF\r\n” command is received.

User can set different output voltages on various channels with different SET commands corresponding to voltage setting on each channel and then update them simultaneously as soon as the external trigger pulse is received (see the example below). Each subsequent write to the channel temporary register overwrites the previous value, so only the last written and stored value is fed to the output register and thus to the output connector.

To read the actual **trigger mode** status it is possible to use the command: “TRG:?\r\n”. The generated reply to this command has the next form: “TRG:ON\r\n” when the “trigger mode” is enabled or “TRG:OFF\r\n” when the **trigger mode** is disabled.

### Example:

TRG example:



SET:CH1:+2.123456\textcolor{red}{r}\textcolor{red}{n} 

ACK\red{r}/\red{n}

SET:CH3:+4.563578\textcolor{red}{r}\textcolor{red}{n} 

ACK ~~r/n~~

*(pause)*

Trigger/Gate pin signal  
(positive edge event )

*Output voltage on the output BNC connector is updated.*

(*pause*)

TRG:OFF $\backslash r \backslash n$

$\text{ACK}_{r/n}$

### 2.2.3 GATE Command

The GATE Command is similar to the TRG Command (see the TRG Command chapter). This command also allows to synchronize the output voltage update with an external event using the signal on the “Trigger/Gate” input connector (see Triggers Connector chapter): the difference respect to the TRG Command is that the start/stop of the acquisition is not triggered by the rising edge of “Trigger/Gate” signal, but it is linked to the “Trigger/Gate” signal level.

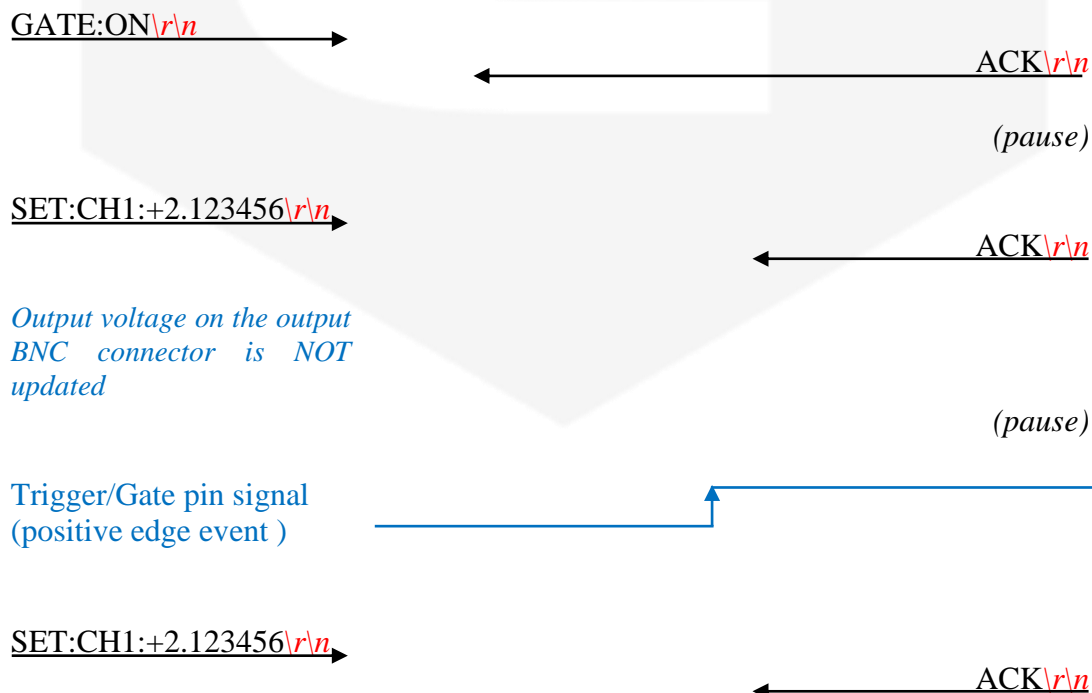
When the PreDAC unit is set to **gate mode** it starts to update the output voltage according to the SET commands. The updating of the output voltage is stopped at the falling edge of “Trigger/Gate”. This mode acts as a set-enabling signal.

A “GATE:ON\r\n” string needs to be sent to the PreDAC in order to set it to “gate mode”. When the command is received the unit replies with an acknowledgement string (“ACK\r\n”). The command that allows to disable the “gate mode” is “GATE:OFF\r\n” (*default*).

To read the actual Gate mode status it is possible to use the “GATE:?\r\n” command. The generated reply to this command has the format of “GATE:ON\r\n” when the **gate mode** is enabled and of “GATE:OFF\r\n” when the **gate mode** is disabled.

#### Example:

*GATE example:*



*Output voltage on the output  
BNC connector is updated  
immediately*

*(pause)*

Trigger/Gate pin signal  
(negative edge event )



SET:CH1:+2.123456\r\n→

← ACK\r\n

*Output voltage on the output  
BNC connector is NOT  
updated*

GATE:OFF\r\n→

← ACK\r\n

## 2.3 Configuration Commands

The commands that can be used to set or to read the PreDAC device configuration are described in this section.

### 2.3.1 STATUS Command

The internal status register of the PreDAC is a monitor of the status of the unit. This register is composed of 2 bytes – i.e. 16 bits – where each byte contains a specific type of information (please note that bit 15 is the MSB and bit 0 is the LSB):

Status Register Structure	
Byte #1 (bits 15 – 8)	Byte #0 (bits 7 – 0)
<b>CONFIGURATION</b> byte	<b>FAULTS</b> byte

The structure of the **CONFIGURATION** byte (bits 15 – 8) of the status register is hereafter presented:

Bit #	Cell caption
15	PreDAC in Slave mode
14	External interlock status (0 – disabled; 1 – enabled)
13	TRIGGER mode (0 – disabled; 1 – enabled)
12	GATE mode (0 – disabled; 1 – enabled)
11	Channel 4 status (0 – OFF, 1 – ON)
10	Channel 3 status (0 – OFF, 1 – ON)
9	Channel 2 status (0 – OFF, 1 – ON)
8	Channel 1 status (0 – OFF, 1 – ON)

The structure of the **FAULTS** byte (bits 7 – 0) is as follows:

Bit #	Cell caption
7	General fault (logical 'OR' of all faults)
6...2	<i>do not care</i>
1	Over-temperature fault (latch of an over-temperature event)
0	External interlock fault (latch of an interlock event)

A brief description of the binary flags in the internal status register of the PreDAC is hereafter presented:

- *PreDAC in Slave mode (bit 15)*: this bit is set when PreDAC is controlled by the BEST system.
- *External interlock enabled (bit 14)*: this bit is set when the external interlock input is enabled (see INTERLOCK Command section);
- *Trigger mode enabled (bit 13)*: this bit is set when the “trigger mode” is enabled (see TRG Command section);
- *Gate mode enabled (bit 12)*: this bit is set when the “gate mode” is enabled (see GATE Command section);
- *Channel Status (bits 11-8)*: these bits indicate if the corresponding output channel is active or it is disabled (it's output voltage is set to 0 V);
- *General fault (bit 7)*: this bit is set if the module has experienced a fault – e.g. generated by an external interlock or an internal protection trip (like internal over-temperature). This bit is a logical ‘OR’ of all other fault flags and it is latching – i.e. when a fault occurs, this bit is set together with the specific fault bit. When a fault is detected, the module switches off all output channels. A status reset of the device is necessary in order to reset the module (see the following section);
- *Over-temperature fault (bit 1)*: this bit is also latching and it is set when the internal PreDAC temperature rises above the 50°C threshold; to reset this flag it is necessary to execute a status reset command (see following section);
- *External interlock fault (bit 0)*: this bit is set when the external interlock signal is enabled and the input interlock signal is high (see Interlock and general I/O connector section); to reset the flag it is necessary to execute a status reset (see the following section).

The internal status register can be read with the “STATUS:?\r\n” command. The reply from the PreDAC unit to this command is in the format “STATUS:value\r\n”, where *value* is the ASCII representation of the internal status register value, composed by 4 hexadecimal digits – corresponding to the 2-byte wide status register (every byte is represented by two hexadecimal digits).

If at least one of the fault conditions occurs, then the respective bit and the general fault bit are set simultaneously. The output voltages are set to a zero voltage level in this conditions and it is not possible to enable them until the internal status register is reset.

The command to reset the fault condition of the status register is “STATUS:RESET\r\n”; the PreDAC unit replies to this command with an acknowledgment string.

**Example:**

STATUS read example:

STATUS:?\r\n →

← STATUS:0181\r\n

STATUS reset example:

STATUS:RESET\r\n →

← ACK\r\n



### 2.3.2 INTERLOCK Command

The PreDAC unit is provided with an external interlock connector that may be connected to an externally generated signal, which can be used to trigger the external interlock fault.

The command to enable or disable the external interlock input is the following: "INTERLOCK:mode\r\n", where *mode* could be "OFF" (default) to disable the interlock input or "ON" to enable it. The unit replies to this kind of command with an acknowledgement string ("ACK\r\n").

In order to read the actual set interlock status it is possible to use the "INTERLOCK:?\r\n" query command.

The generated reply to this command has the format "INTERLOCK:mode\r\n", where *mode* could be:

- OFF if the interlock input is disabled (default);
- ON if interlock input is enabled.

#### Example:

INTERLOCK set example:

INTERLOCK:ON\r\n → ← ACK\r\n

INTERLOCK read example:

INTERLOCK:?\r\n → ← INTERLOCK:ON\r\n

### 2.3.3 TEMP command

TEMP Command (“TEMP:?*r**n*”) allows user to read temperature from the internal temperature sensor. Temperature value is updated every 10 seconds.

If temperature rises over the threshold of 50°C, the over-temperature fault trips and the output voltages are set to 0 V level. After a fault event occurs it is necessary to reset the internal status register in order to be able to reactivate voltage outputs.

The reply to the TEMP command is in the format “TEMP:*value**r**n*”, where *value* is the integer temperature readback value (in [°C]).

**Example:**

TEMP read example:

TEMP:?*r**n* → ← TEMP:28*r**n*

### 2.3.4 VER Command

The “VER:?\r\n” command returns information about the PreDAC unit and the currently installed firmware version.

The reply to the “VER\r\n” command is in following format:

VER:*model*:*ver*:*channels*\r\n

where:

- *model* is a string indicating the device - i.e. “PREDAC”;
- *ver* contains the string corresponding to the installed firmware version;
- *channels* is a string indicating the number of installed channels – i.e. DACs.

**Example:**

VER example:

VER:?\r\n → VER:PREDAC:0.9.81:3CHN\r\n

The “PREDAC” device of the previous example has the “0.9.81” firmware version installed and it has a 3 output channels.

### 2.3.5 HWRESET Command

The “HWRESET\r\n” command performs a complete reset of the hardware and firmware on the on-board FPGA, thus re-initializing the entire PreDAC module control electronics.

The unit replies with an acknowledgment string (“ACK\r\n”) before resetting the module.

**Example:**

HWRESET *example:*

HWRESET\r\n → ACK\r\n

### 2.3.6 ID Command

The “ID:?*r*\n” command returns the pre-assigned PreDAC identification name as a string.

The reply from the PreDAC contains the value stored in the module EEPROM and it assumes the following format:

ID:*module\_id*\n

where:

- *module\_id* is the module identification name stored in non-volatile memory as an ASCII string.

The ID command, being a reading command, returns a response in any module condition.

#### **Examples:**

*ID example with the module identification “Actuator1”:*

ID:?*r*\n



ID:ACTUATOR1\n



### 2.3.7 IDSET Command

Users can write a desired identification name in the module EEPROM with the IDSET command. This name can be read using the “ID” command described previously in this document.

The correct format for this command is as follows:

IDSET:*module\_id*\r\n

where:

- *module\_id* is the ASCII content to be written to the EEPROM.

Replies from the PreDAC are in the form “ACK\r\n” or “NAK\r\n”; this non-acknowledgment reply is generated when the *module\_id* string length is greater than 32 bytes – i.e. 32 characters.

#### **Examples:**

*IDSET example, the new identification name is Actuator1:*

IDSET: Actuator1\r\n

ACK\r\n

### 2.3.8 RES Command

The RES command is used to change the resolution of the output voltage, which can be of 21 bits (high-resolution) or of 16 bits (standard).

If resolution is set to 21 bits then dithering is enabled while is disabled when the resolution is set to 16 bits.

The correct form format for this command is as follows:

RES:*resolution*\r\n

where:

- *resolution* can be a value of 16 (16-bit setting) or of 21 (21-bit setting).

Replies from the PreDAC unit are in the form “ACK\r\n” or “NAK\r\n”; this non-acknowledgment reply is generated when the resolution selection is not a valid one (not 16 nor 21).

The command “RES:?\r\n” can be used to read the actual set output resolution. The generated reply to this command has the next form: “RES:*resolution*\r\n”, where *resolution* could be “21” (*default*) if the resolution is set to 21 bits or “16” if the resolution is set to 16 bits.

#### Examples:

*RES example with an incorrect value:*

RES:20\r\n → NAK\r\n

*RES example with the valid parameter setting:*

RES:21\r\n → ACK\r\n

## 2.4 Command Table Summary

Command	Purposes	Parameters
<b>GATE</b>	Enable gate output voltage update	<b>ON</b>
	Disable gate output voltage update	<b>OFF</b>
<b>HWRESET</b>	Perform a hardware and firmware reset	<b>/</b>
<b>ID</b>	Query identification name	<b>?</b>
<b>IDSET</b>	Set identification name	<b>module_id</b>
<b>INTERLOCK</b>	Enable external interlock input	<b>ON</b>
	Disable external interlock input	<b>OFF</b>
	Query interlock setting	<b>?</b>
<b>RES</b>	Set output voltage resolution	<b>resolution</b>
	Query resolution setting	<b>?</b>
<b>SET</b>	Set output voltage on the channel #y	<b>CHy:value</b>
	Set zero output voltage on the channel #y	<b>CHy:OFF</b>
	Query set voltage on the channel #y	<b>CHy:?</b>
	Set output voltage on all channels	<b>ALL:value</b>
	Set zero output voltage on all channels	<b>ALL:OFF</b>
<b>STATUS</b>	Query device status	<b>?</b>
	Reset status fault conditions	<b>RESET</b>
<b>VER</b>	Query the device firmware version	<b>?</b>
<b>TEMP</b>	Read the devices internal temperature	<b>?</b>
<b>TRG</b>	Enable triggered output voltage update	<b>ON</b>
	Disable triggered output voltage update	<b>OFF</b>



## 3. Ethernet Communication

The communication with the PreDAC unit is based on a 10/100/1000 Mbps Ethernet link. The suggested connection speeds are 100 Mbps or 1 Gbps since the 10 Mbps connection represents a limit to the transmission data rate.

The factory network configuration and the **CAENels Device Manager** software are described in the following sections.

### 3.1 IP Address Assignment

The device is shipped with default IP address, subnet mask, gateway and TCP-IP communication port:

Parameter	Factory value
<i>IP address</i>	<b>192.168.0.10</b>
<i>Subnet mask</i>	<b>255.255.255.0</b>
<i>Gateway</i>	<b>192.168.0.1</b>
<i>TCP/IP port</i>	<b>10001</b>

Even if the PreDAC device can be connected to a LAN network, a point-to-point Ethernet connection is strongly recommended in order to obtain minimum delay, maximum data rate performance and to avoid possible communication problems – i.e. increasing communication reliability. This implies that the host PC and the PreDAC should reside on the same Ethernet subnet.



For a point-to-point connection it is not necessary to use a twisted cable because the used Ethernet link has an automatic detection of the communication direction – i.e. auto-sensing capability.

To change the device network setup it is necessary to use the **CAENels Device Manager** software that can be downloaded from the CAENels website [www.caenels.com](http://www.caenels.com). A briefly description of this software is given in next section.

## 3.2 CAENels Device manager

The software **CAENels Device manager** can be used to search for all the PreDAC devices connected to the local network and to configure them. This software also allows to set the network configuration of the found devices and to update their firmware.

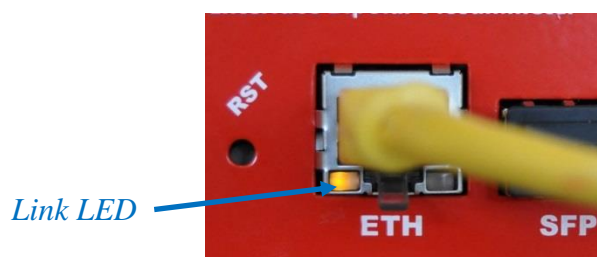
The **CAENels Device manager** is available for Windows and Linux platform and the system requirements hereafter listed:

-  Windows minimum system requirements
  - Windows® XP or newer
  - Intel® or equivalent processor
  - 70 MB available HD space
  - Ethernet network card
-  Linux minimum system requirements
  - Linux kernel 2.2.x or newer
  - Intel® or equivalent processor
  - 70 MB available HD space
  - Ethernet network card

### 3.2.1 Searching for connected devices

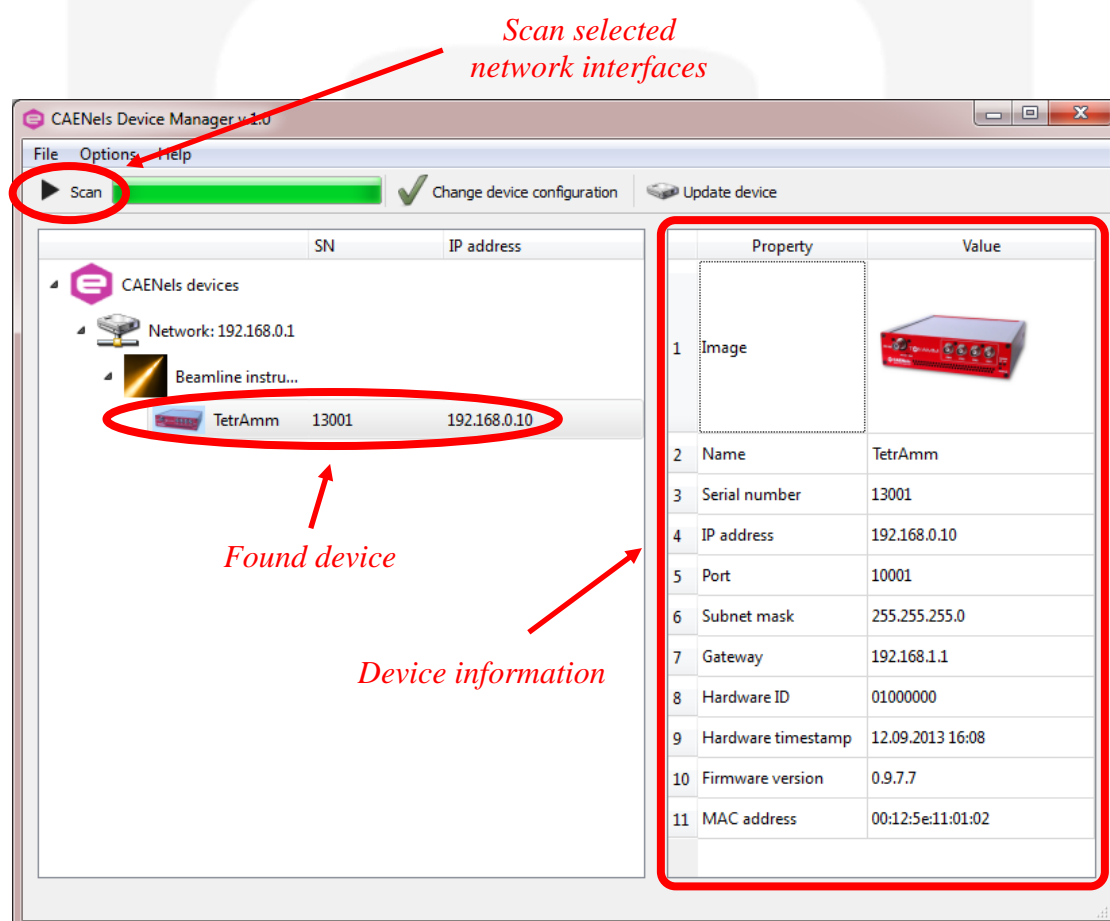
Please follow the next steps in order to search for the PreDAC devices connected to the local network:

- connect the host PC and the PreDAC directly with an Ethernet cable (or through a network);
- verify that the “*Link LED*” on the RJ45 connector is turned on (**amber** for a 1 Gbps connection as shown in **Figure 4** or **green** for a 100 Mbps connection). The LED is turned off if the Ethernet cable is not connected or if the speed of connection is limited to 10 Mbps (in this last case the device is working correctly even if it is not recommended to use a slow connection since the data transfer rate is limited);



**Figure 4:** Ethernet Link

- connect the PreDAC to the AC/DC power supply unit and switch it on;
- install and launch the **CAENels Device manager** software;
- perform a scan to discover the connected PreDAC devices by clicking the “Scan” button as indicated in **Figure 5**. If there are multiple available networks it is possible to select the network/networks to be scanned in the “Selected network interfaces” window available under the “Options” menu. All the information about the selected devices is shown in the right side of the main window.



**Figure 5:** Main interface

If you have a firewall enabled on your router or on your computer, please make sure that the firewall is not preventing communication between your computer and the PreDAC device.

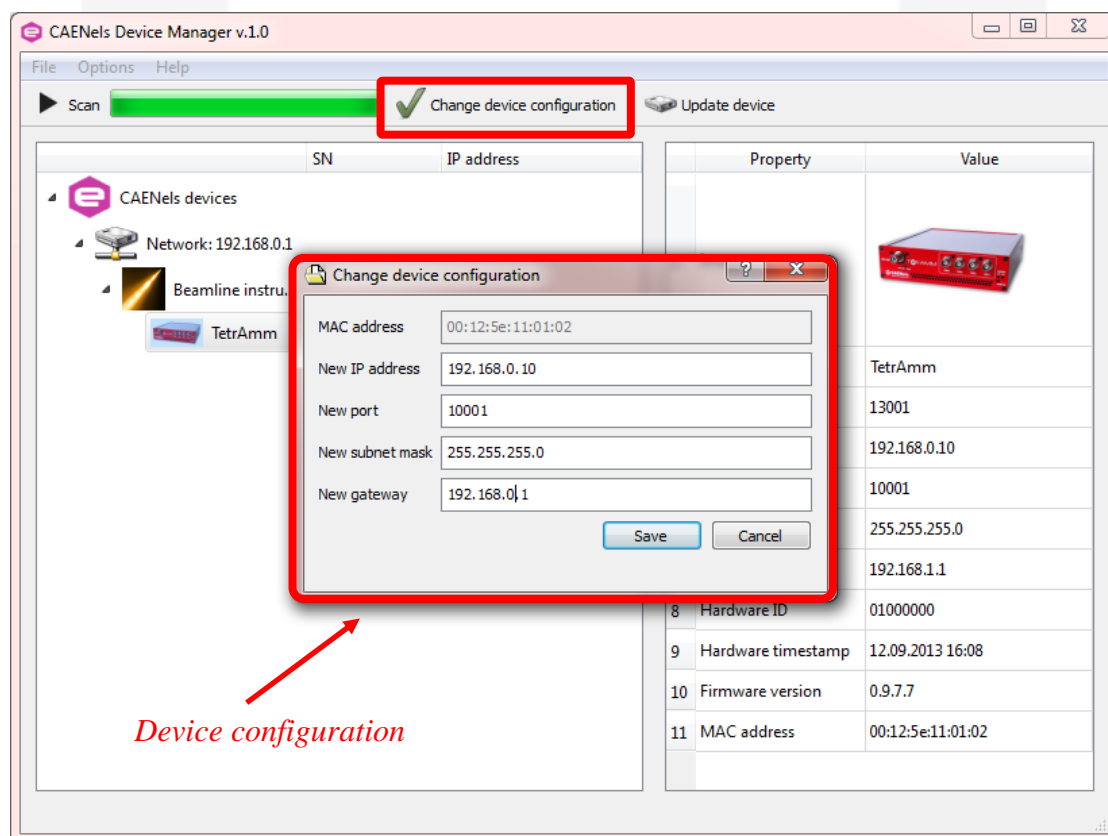
The **CAENels Device manager** uses **UDP port 30719** to find the device, so make sure that the UDP traffic is allowed in both directions on that specific port.

### 3.2.2 Device Configuration

It is possible to change the Network configuration of the found devices. In order to set the Network configuration it is necessary to select the desired device and to click on the “*Change device configuration*” button in the main window as shown in **Figure 6**. The configurable Network options are:

- Device IP address;
- TCP/IP communication port;
- Subnet mask;
- Gateway.

To apply the changes on the device configuration it is necessary to edit the corresponding fields and then to click on the “*Save*” button. A screenshot of a sample device configuration is shown in the following picture:

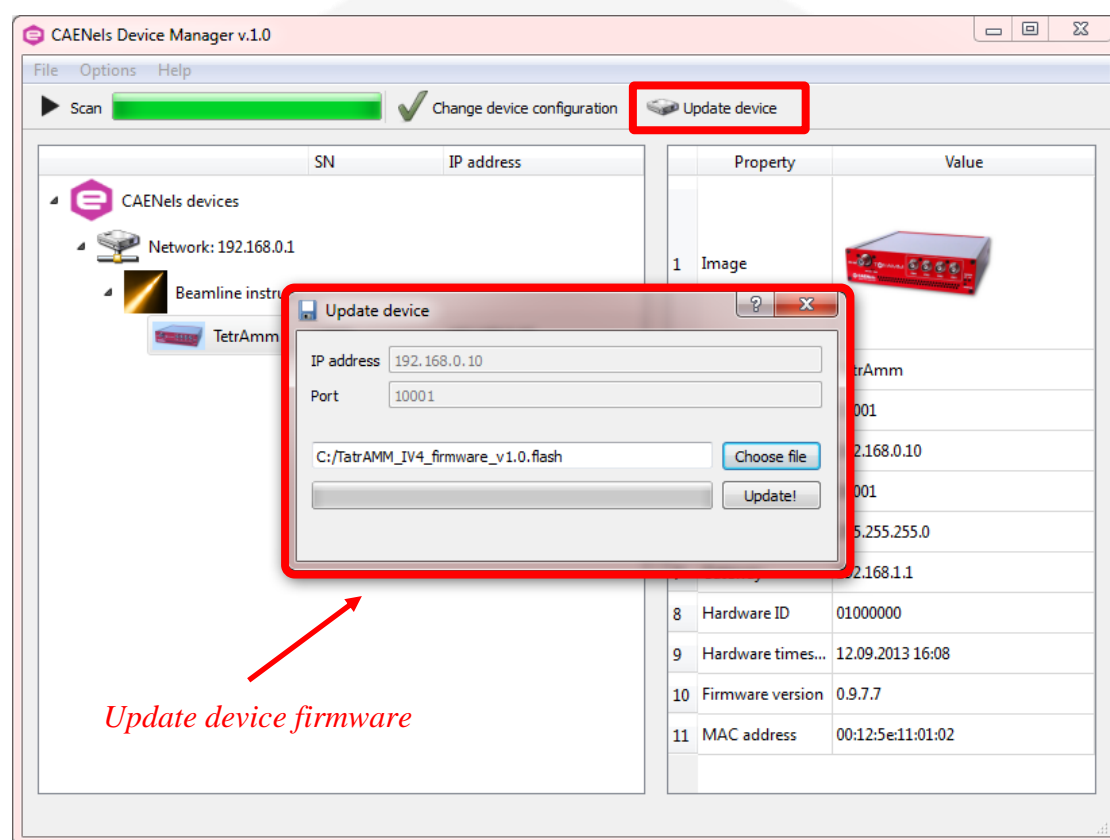


**Figure 6:** Change device configuration

### 3.2.3 Firmware Upgrade

The **CAENels Device manager** software also allows remotely updating the firmware of the PreDAC devices. Once the desired device is found, it is possible to perform the firmware update by clicking on the “*Update device*” button as shown **Figure 7**. The new opened window allows to select the new firmware file (*Flash file - \*.flash*).

Once the flash file has been selected it is possible to start the firmware update by clicking the “*Update!*” button. The firmware update task will take a few minutes. A screenshot of the update menu is shown hereafter:



**Figure 7:** Update device

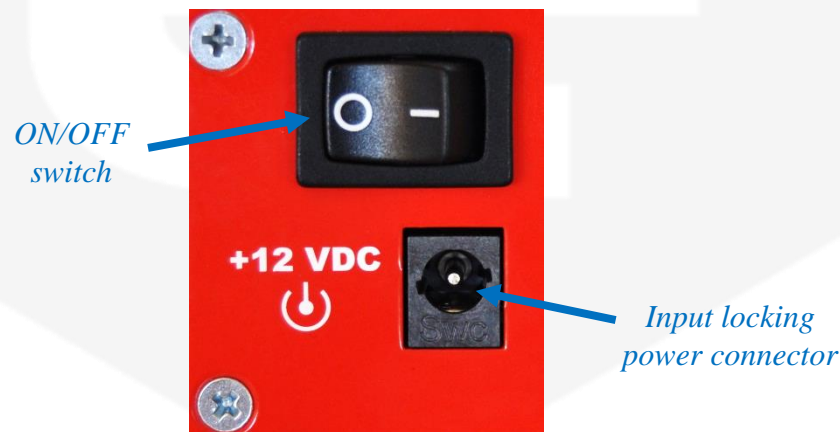
## 4. I/O Connectors

This chapter describes the I/O connectors present on the device front and rear panels, their corresponding pinout and each signal functionality.

### 4.1 Power Connector

The input power connector is a standard male locking jack socket. The input voltage is rated at +12V ( $\pm 3\%$ ) with a maximum input current of 1A.

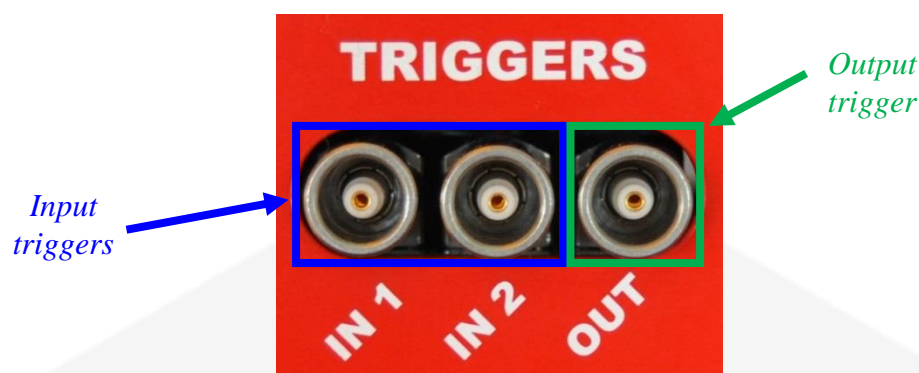
The input ON/OFF switch is placed above the input power connector which allows turning ON or OFF the device. The used connector is shown in **Figure 8**:



**Figure 8:** Power connector and switch

## 4.2 Triggers Connector

The PreDAC device has two input and one output trigger signals on LEMO coaxial connectors. These input/output connectors are called “*Triggers*” and are placed on the rear panel of the device as shown in **Figure 9**:



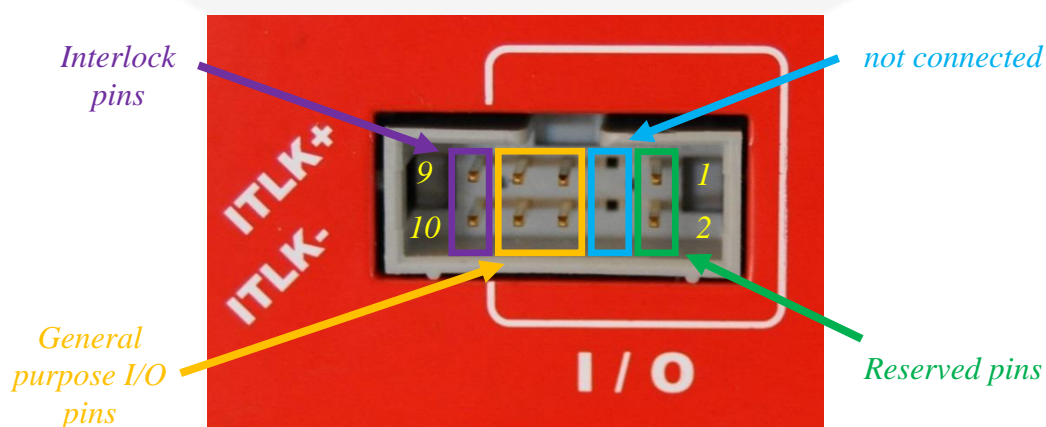
**Figure 9:** “*Triggers*” connectors on rear panel

Signal levels are TTL, LVTTTL and CMOS compatible. The maximum rated output current is 24mA.

The “*IN 1*” input is also called “*Trigger/Gate*” signal and it is used to synchronize the update of output voltage of the device to an external event (for more information please refer to TRG Command and GATE Command sections). The “*IN 2*” and “*OUT*” connectors are reserved for future uses.

## 4.3 Interlock and general I/O connector

The “Interlocks and general I/O” connector, that has the pinout configuration described in **Figure 10**, is present on the rear panel of the PreDAC unit:



**Figure 10:** Interlock and I/O connector

The pin functions are summarized in the next table:

Pin #	Function
1-2	Reserved pins
3-4	<i>not connected</i>
5-8	General purpose I/O pins
9-10	External interlock pins

The “*External interlock pins*” (pins 9-10) can be used to detect an external signal that can be used to trigger the external interlock fault and to switch off the High Voltage module (see INTERLOCK Command and STATUS Command Commands sections for more information). The interlock pins are galvanically isolated from ground.

The maximum voltage that can be applied to the interlock terminals is rated at **+24V** (the minimum signal that guarantees the tripping of this interlock is rated at +3V); the maximum reverse voltage that this interlock can sustain is rated at -5.5V.

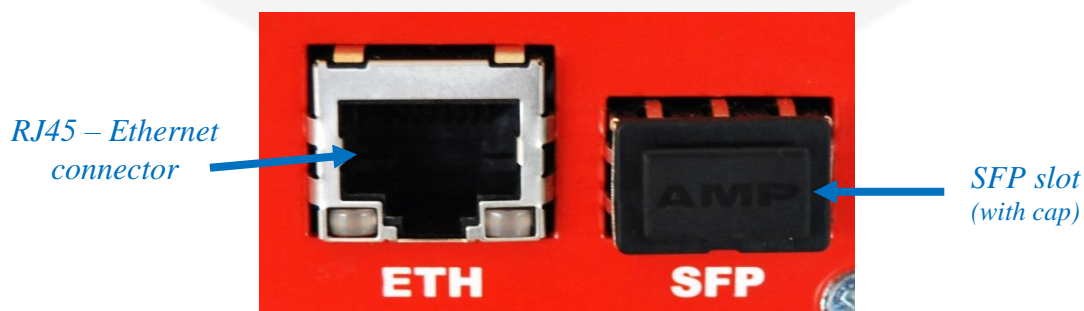
The “*General purpose I/O pins*” (pins 5-8) are connected to the internal digital section and they are reserved for future system updates.

The “*not connected pins*” (pins 3-4) are not present or if present, they are not connected to the internal digital system.

The “*Reserved pins*” (pins 1-2) are connected to the internal digital section and are reserved for internal use, so they must NOT be connected.

## 4.4 Ethernet and SFP connector

On the rear side of the PreDAC unit there are also a RJ45 Ethernet connector and a small form-factor pluggable (SFP) slot as indicated in **Figure 11**:



**Figure 11:** Ethernet and SFP connections

The RJ45 Ethernet slot is used to communicate with PreDAC unit. The connector is linked to a true 10/100/1000 Mbps physical device. For more information about the Ethernet communication see the Ethernet Communication section.



The SFP slot allows connecting a copper or optic platform to the internal digital system with a fixed speed of 1 Gbps and it is reserved for the integration of the PreDAC into the **BEST** – Best Enhanced Stabilization Technology system for the photon beam optimization and stabilization.

## 4.5 Output BNC connectors

The up to four, with a default configuration of two, BNC connectors (Bayonet Neill-Concelman) on the front panel of the PreDAC unit are used to supply the output voltages. The BNC connectors are miniature quick connect/disconnect RF connectors mainly used for coaxial cables.

Channel incremental numbering, as can be seen in **Figure 12**, is right-to-left (OUT1 is the one on the right side while OUT4 is the one on the left):



**Figure 12:** output BNC connectors (default 2-channel configuration)

**The PreDAC unit has to be placed next to the piezo power driver (e.g. power amplifier) in order to reduce cable lengths and thus cable capacitance and to minimize consequent noise pick-up.**

## 5. Technical Specifications

Main technical specifications for the PreDAC unit are shown in the following table:

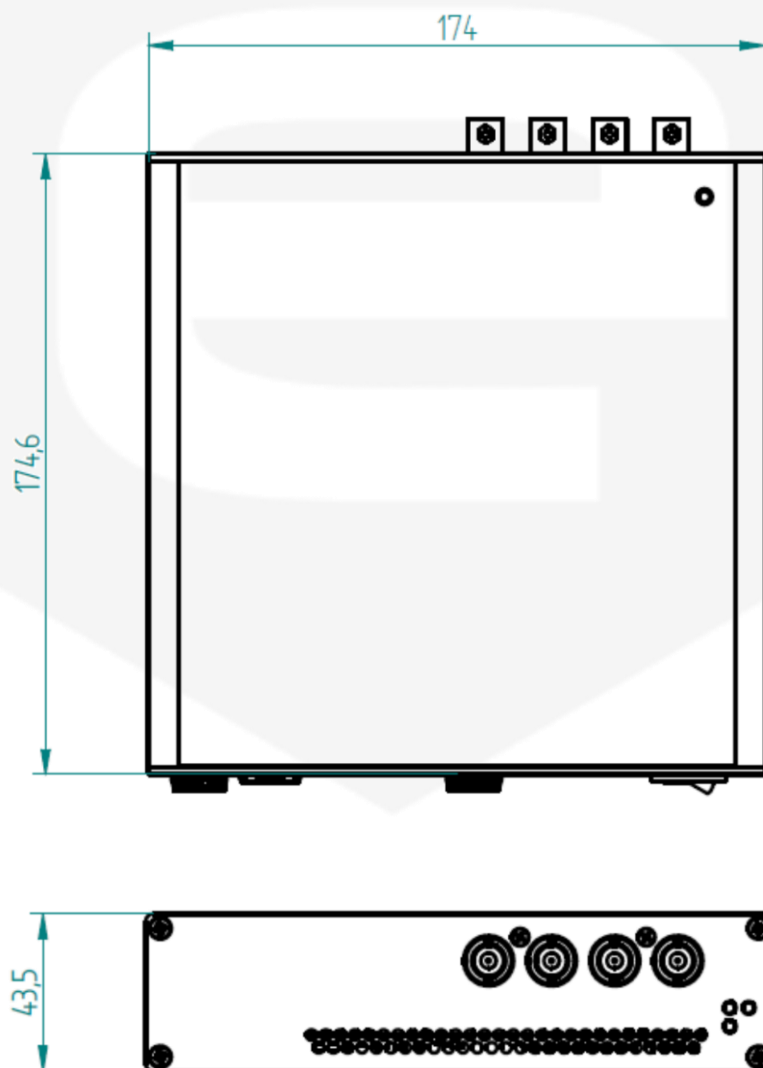
Characteristic	Value
Output Channels	up to 4 (default is 2)
Output Voltage Range	$\pm 12$ V
Output Voltage Resolution	21 bits or 16 bits
Output Voltage Polarity	Bipolar
Analog Bandwidth – BW	10 kHz
Output Voltage Accuracy	12 $\mu$ V
Output Voltage Noise	ppm/FS
Output Impedance	50 $\Omega$
Maximum Output Current	10 mA
Rise and Fall time (10-90%)	35 $\mu$ s
Update rate	Up to 100 ksamples/s/ch
Communication	Ethernet 10/100/1000 TCP-IP
Extra Communication interface	SFP – Small form-factor pluggable for <b>BEST</b> integration
External Signals	Configurable Trigger/Gate External Interlock
Fault condition	External interlock Internal over-temperature
Output connectors	BNC

Additional Features	Firmware remote update External interlock protections
Input Voltage Supply ( $\pm 3\%$ )	+12 V
Dimensions	195 x 173 x 45
Weight	850 g



## 6. Mechanical Dimensions

The mechanical dimensions of the PreDAC unit, including connectors, are hereafter presented in **Figure 13**:



**Figure 13:** PreDAC mechanical dimensions

## 7. PreDAC Power Supply

This chapter describes the general characteristics and the main features of the TetrAMM linear power supply called PS1112. This power supply is particularly designed for operation with the CAENels TetrAMM picoammeter.

### 7.1 The PS1112 Linear Power Supply

CAENels PS1112 is a single-output +12V linear power supply designed for low-noise operation and it is especially suited for low power measurement system where switching power supplies could corrupt measuring accuracy, precision and noise.

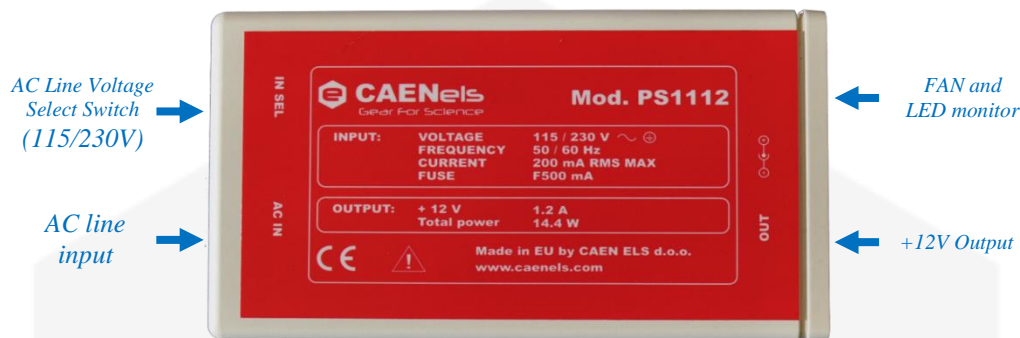
The power supply is housed in a light, robust and compact plastic box (refer to **Figure 14**~~Error! Reference source not found.~~) that can be placed next to the supplied device in order to reduce cable lengths and minimize consequent possible noise pick-up.



**Figure 14:** PS1112 linear power supply

## 7.2 The PS1112 at a Glance

The PS1112 is an isolated unipolar linear power supply with one output connector. The PS1112, its input, output, indicators and switches are shown in **Figure 15**:



**Figure 15:** PS1112 connections

The AC Power Line input and the AC Line Voltage selection switch (115/230V) are placed on one side of the box; the output connector, the LED monitor and the air outlet on the other one.

The AC Power Line input is also equipped with an integrated two-slot fuse holder (one active and one as a replacement).

The PS1112 has an isolated output voltage of +12V rated at 1.2A maximum output current.

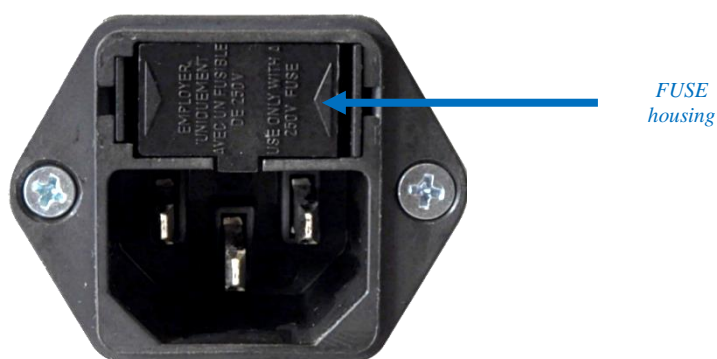
## 7.3 I/O Connectors

This chapter describes the I/O connectors and switches, their corresponding pinout and their functionality.

### 7.3.1 AC Line Input Connector

The AC Line Input connector is in a standard VDE format and it is provided with a two-slot fuse holder for over-current (e.g. short-circuit) protection.

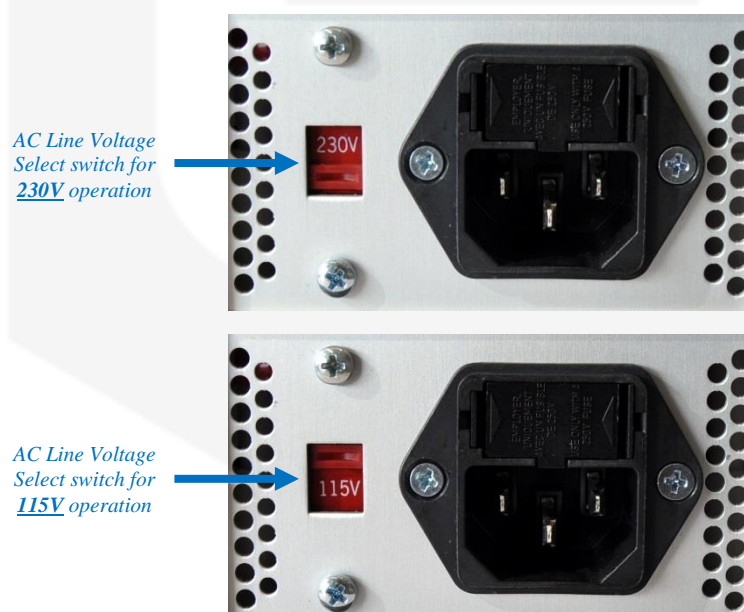
The PS1112 power supply is designed for 115/230V input voltage and for 50-60 Hz input frequency operation: the correct AC input voltage rating **MUST** be selected by the user using the AC Line Voltage Select switch placed next to the VDE plug (i.e. on the left side) before connecting the power supply to the mains. The fuse is housed over the VDE plug as indicated in **Figure 16**:



**Figure 16: AC input and fuse housing**

### 7.3.2 AC Line Voltage Select Switch

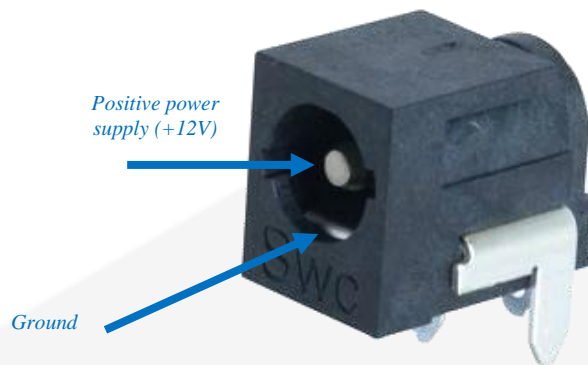
The PS1112 linear power supply can be used either with a 115V – 60Hz AC power line (e.g. United States) or with a 230 V – 50 Hz AC Line (e.g. Europe); be sure to select the correct input voltage rating by switching the AC Line Voltage Select switch placed on one side of the box. Possible switch positions, one for each input voltage rating, are shown in the following **Figure 17** (230V and 115V respectively):



**Figure 17: AC line voltage select switch**

### 7.3.3 Output Connectors

The power supply has one locking output connector indicated as “OUT”. The central pin corresponds to the positive power supply (+12V) respect to the external conductor that is connected to its ground (refer to **Figure 18**).



**Figure 18:** TetrAMM mechanical dimensions

### 7.3.4 Cabling

The PS1112 linear power supply is equipped with a female to female locking power plug cable in order to handle connections to the CAENels TetrAMM device. The standard cable length is 1.5m (60").

## 7.4 Technical Specifications

Main technical Specifications for the PS1112 linear power supplies are presented in the following table:

Characteristic	Value
Output Voltage	+12 V
Maximum Output Power	14.4 W
Maximum Output Current	1.2 A
AC Line Voltage Input	115V / 230 V
AC Line Frequency	50 / 60 Hz
Dimensions	115 x 95 x 57 mm
Weight	850 g
Indicators	1 LED (OUT OK)
Cooling	Forced air convection (integrated)
Fuse	F500 mA



## 8. Appendix

8

### 8.1 List of the Error Codes

The PreDAC unit replies with a Not AcKnowledge (“NAK”) if the received command is not correct or it is not accepted. This “NAK” reply is followed by a two digit “error code” field, which indicates the error cause and/or type. The list of the possible error codes is hereafter presented:

Error Code	Error name	Brief description of error
<b>00</b>	<b>Invalid command</b>	<i>Command field is not valid; the list of valid commands is shown in the Command Table Summary section</i>
<b>10</b>	<b>Wrong SET command channel parameter</b>	<i>Given parameter is not allowed SET command channel setting (see SET Command)</i>
<b>11</b>	<b>Wrong SET command value parameter</b>	<i>Given parameter is not allowed SET command value setting (see SET Command)</i>
<b>12</b>	<b>Wrong TRG command parameter</b>	<i>Given parameter is not allowed TRG command setting (see TRG Command)</i>
<b>13</b>	<b>Wrong GATE command parameter</b>	<i>Given parameter is not allowed GATE command setting (see GATE Command)</i>
<b>14</b>	<b>Wrong USRCORR field parameter</b>	<i>Given parameter is not allowed USRCORR command field setting (see <b>Error! Reference source not found.</b>)</i>
<b>15</b>	<b>Wrong USRCORR value parameter</b>	<i>Given parameter is not allowed USRCORR command parameter setting (see <b>Error! Reference source not found.</b>)</i>
<b>16</b>	<b>Wrong STATUS command parameter</b>	<i>Given parameter is not allowed STATUS command setting (see STATUS Command)</i>

<b>17</b>	<b>Wrong INTERLOCK command parameter</b>	<i>Given parameter is not allowed INTERLOCK command setting (see INTERLOCK Command)</i>
<b>18</b>	<b>Wrong TEMP command parameter</b>	<i>Given parameter is not allowed TEMP command setting (see TEMP command)</i>
<b>19</b>	<b>Wrong VER command parameter</b>	<i>Given parameter is not allowed VER command setting (see VER Command)</i>
<b>20</b>	<b>Wrong ID command parameter</b>	<i>Given parameter is not allowed ID command setting (see ID Command)</i>
<b>21</b>	<b>Wrong IDSET command parameter</b>	<i>Given parameter is too long (see IDSET Command)</i>
<b>22</b>	<b>Wrong RES command parameter</b>	<i>Given parameter is not allowed RES command setting (see RES Command)</i>
<b>50</b>	<b>PreDAC in slave mode</b>	<i>PreDAC is controlled by the BEST system and it cannot receive additional user commands</i>